AMENDMENTS TO THE CLAIMS

Please amend claims 1, 2, 7, 14 and 15 as follows:

1. (Currently Amended) A video data transfer system comprising:

a real time output path through which video data processed by a video processor is sent to a display via a frame buffer;

a capturing path which is independent of said real time output path and through which said video data is sent to a system memory via a system bus and not through the frame buffer; and

a gate in said capturing path, said gate being controllable to permit said video data to pass when received from said video processor, wherein a rate at which said video data is sent to the display is unaffected by passage of said video data through said capturing path.

2. (Currently Amended) A video data transfer system, comprising:

a real time output path through which video data processed by a video processor is sent to a display via a frame buffer;

a capturing path which is independent of said real time output path and through which said video data is sent to a system memory via a system bus and not through the frame buffer, wherein

said real time output path comprises:

an off-screen memory which receives video data from said video processor via a data bus and stores video data therein, said off-screen memory being in the frame buffer; and

a display control circuit which receives video data read from said off-screen memory via said data bus for enlargement and interpolation processing and transfers processed results to said display, and wherein

said capturing path comprises:

a gate which is opened only when video data is received from said video processor for capturing; and

memory means for storing said video data sent through said gate and for transferring said video data to said system bus, wherein a rate at which said video data is sent to the display is unaffected by passage of said video data through said capturing path.

3. (Previously Presented) A video data transfer system as defined in claim 2, wherein

said memory means transfers said stored video data to said system bus when said system bus is not occupied by some other unit and, when said system bus is occupied by some other unit, checks if said stored data contains a field delimiter or a frame delimiter and closes said gate to stop data transfer when said stored data contains the delimiter and, when said stored data does not contain the delimiter, stores the next video data passing through said gate.

4. (Previously Presented) A video data transfer system as defined in claim 1, further comprising:

a capture path memory in said capturing path;

said capture path memory being connected to said gate; and

said capture path memory being operable to store said video data passed by said gate.

5. (Previously Presented) A video data transfer system as defined in claim 4, wherein said capture path memory is further effective to transfer said video data to said system bus.

6. (Previously Presented) A video data transfer system as defined in claim 5, wherein said real time output path further comprises:

an off-screen memory effective to receive said video data from said video processor via a data bus and store said video data therein; and wherein

said off-screen memory is in said frame buffer.

7. (Currently Amended) A video data transfer method, comprising:

providing video data from a video processor to a plurality of paths independent of each other;

sending said video data to a display through a frame buffer in at least one of said independent paths operating as a real time output path;

sending said video data to a system memory through a system bus and not through the frame buffer in at least another of said independent paths operating as a capture path; and

controlling said capture path to permit said video data to pass to said system memory when said video data is to be captured, wherein a rate at which said video data is sent to the display is unaffected by passage of said video data through said capture path.

8. (Previously Presented) A video data transfer method as defined in claim 7, further comprising storing said video data in a capture path memory in said capture path when said video data is permitted to pass to said system memory.

9. (Previously Presented) A video data transfer method as defined in claim 8, further comprising checking said system bus for occupation by other devices connected thereto.

10. (Previously Presented) A video data transfer method as defined in claim 9, further comprising transferring said video data from said capture path memory to said system memory when said system bus is not occupied by other devices connected thereto.

11. (Previously Presented) A video data transfer method as defined in claim 10, further comprising checking said video data stored in said capture path memory for at least one of a field and a frame delimiter when said system bus is occupied.

12. (Previously Presented) A video data transfer method as defined in claim 11, further comprising controlling said capture path to prevent said video data from being stored in said capture path memory when said capture path memory contains said at least one of a field and a frame delimiter.

13. (Cancelled).

14. (Currently Amended) A method of transferring video data, the method comprising:

receiving video data;

determining whether the video data is to be captured;

processing the video data to produce processed data;

forwarding the processed video data to a first path, the first path including a display control circuit and a frame buffer; and

forwarding the processed video data to a second path when the determining indicates that the video data is to be captured, the second path not including the frame buffer;

wherein the first and second paths are distinct, and wherein a rate at which the video data is sent to a display controlled by the display control circuit is unaffected by passage of the video data through the second path.

15. (Currently Amended) A video data transfer system comprising:

a video processor which receives video data and processes the video data to produce processed video data;

a display path coupled to the video processor, the display path including a frame buffer, the display path conveys the processed video data from the video processor to a display; and

a capturing path coupled to the video processor, the capturing path conveys the processed data from the video processor to a system memory, the capturing path not including the frame buffer, the capturing path being distinct from the display path, wherein a rate at which said video data is sent to the display is unaffected by passage of said video data through said capturing path.